

Serial No.: 08/082,328

REMARKS

In the Office Action of October 23, 2002:

Claims 44, 102, 143, 144, 146, 147 and 217-222 were allowed.

Claims 43, 46-48, 52 and 213-216 were objected to as being dependent upon a rejected base claim but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 28, 37-39, 41, 42, 53-55, 58, 59, 210-212, 223 and 224 were rejected under 35 U.S.C. 102(e) as being anticipated by Koepf, USP 5,138,436.

Claim 28 was rejected under 35 U.S.C. 103(a) as being unpatentable over Moresco et al., USP 5,404,265.

Claims 40, 45, 56 and 57 were rejected under 35 U.S.C. 103(a) as being unpatentable over Koepf.

Applicants' invention relates to apparatus for communicating or signalling between integrated circuit (IC) chips, modules or substrates using capacitive coupling rather than conductive paths. For example, in large part, the need for multichip modules arises from the inability of the prior art to produce arbitrarily large semiconductor dies with acceptable yield as well as the high cost of wiring on semiconductor dies. Such problems have forced designers to partition large systems among multiple dies. To effect signalling between different chips and modules, the prior art requires the use of conductive connectors, solder bumps, wire-bond interconnections or the like. Unfortunately, such means introduces significant latency, frequency limitations and power requirements. To mitigate these problems, the present invention effects signalling capacitively. As described beginning at page 25, line 16, pairs of half-capacitor plates (Fig. 1, elements 13, 14), one half located on each IC chip (11), module or substrate (10), are used to capacitively couple signals from one IC chip, module or substrate to another. The use of such plates relaxes the area needed to effect signalling, and reduces or eliminates the requirements for exotic metallurgy.

In one embodiment of applicants' invention shown in Fig. 2, signals are capacitively coupled across a pair of coupled half-capacitors 13 between a pair of transmission lines 34 and 37 on die 11 and a pair of transmission lines 32 and 33 on substrate 10. Transmission lines 32 and 33 are terminated by termination resistors 31b and 31c connected to a ground plane 31a in substrate 10. By locating the ground plane in or on the substrate, applicants are able to take advantage of existing technologies for manufacturing high quality substrates having uniform electrical properties such as printed wiring boards, flex circuit boards and multi-chip modules.

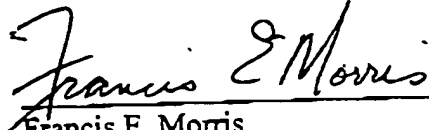
Koepf describes an interconnect package for use with a monolithic microwave integrated circuit (MMIC). As the Examiner notes, Fig. 4 of Koepf discloses a chip 18, an interconnect substrate 28, a capacitive connection between the chip and the substrate, and signal leads, microstrip line 52 and RF transmission line 31, on the chip and substrate,

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Aside from the fee for the petition for extension of time, no additional fee is believed due for filing this response. However, if a fee is due, please charge such fee to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

Date: April 23, 2003


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APPENDIX A

SUMMARY OF CLAIMS

Claim 1 (currently amended)
Claims 2-27 (canceled)
Claim 28 (currently amended)
Claims 29-36 (canceled)
Claims 37-43 (original)
Claim 44 (allowed)
Claim 45 (original)
Claim 46 (previously amended)
Claims 47-48 (original)
Claims 49-51 (canceled)
Claim 52 (currently amended - rewritten in independent form)
Claim 53 (previously amended)
Claims 54-58 (original)
Claim 59 (currently amended)
Claims 60-101 (canceled)
Claim 102 (allowed)
Claims 103-142 (canceled)
Claims 143-144 (allowed)
Claim 145 (canceled)
Claims 146-147 (allowed)
Claims 148-209 (canceled)
Claims 210-216 (original)
Claims 217-222 (allowed)
Claim 223 - (currently amended)
Claim 224 (original)